VLSI Fixed-Outline Floorplanning using Convex/Nonconvex Model

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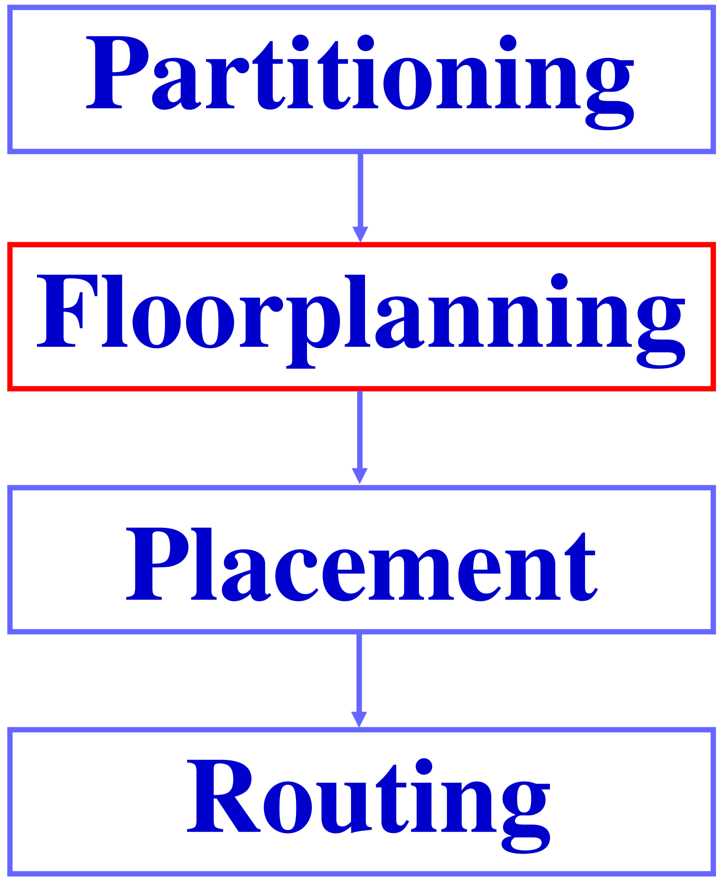
Outline

- Introduction
- Background
  - Classical (outline-free) floorplanning
  - Fixed-outline floorplanning
- Mathematical Programming Model
  - Convex version Attractor-Repeller model
  - A two-stage optimization methodology
- Implementation and Experiments
- Conclusions

Circuit Layout Cycle

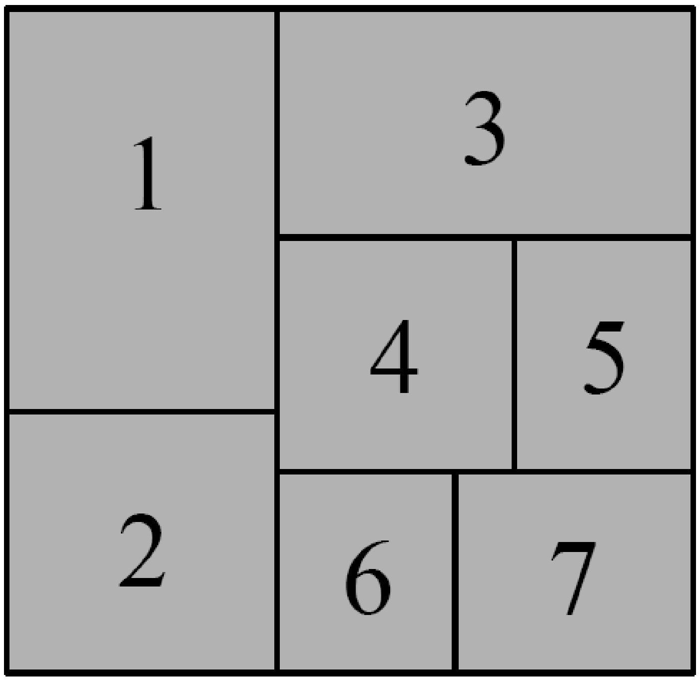


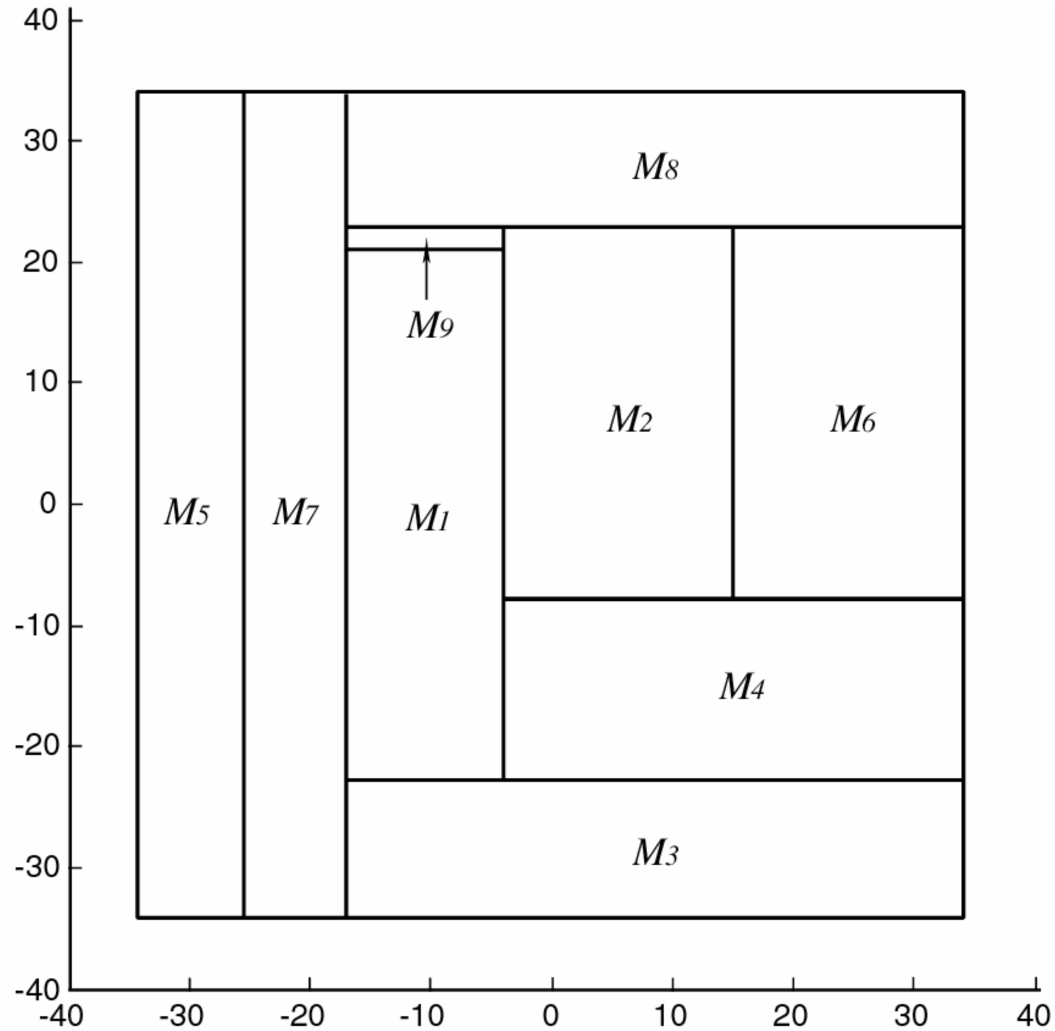
Floorplanning

Floorplanning

- Floorplanning is the placement of soft modules, which have fixed areas but unknown dimensions.
- Floorplanning determines module positions to optimize the circuit performance by minimizing wire length.

Floorplanning





Convex Optimization Model

- **Clique model**
- **Target distance**
- **Convex AR model**
- **A two-stage optimization methodology**
- **Proposed by *Etawil et. al, 1999* and improved by *Anjos and Vannelli, 2004*.**

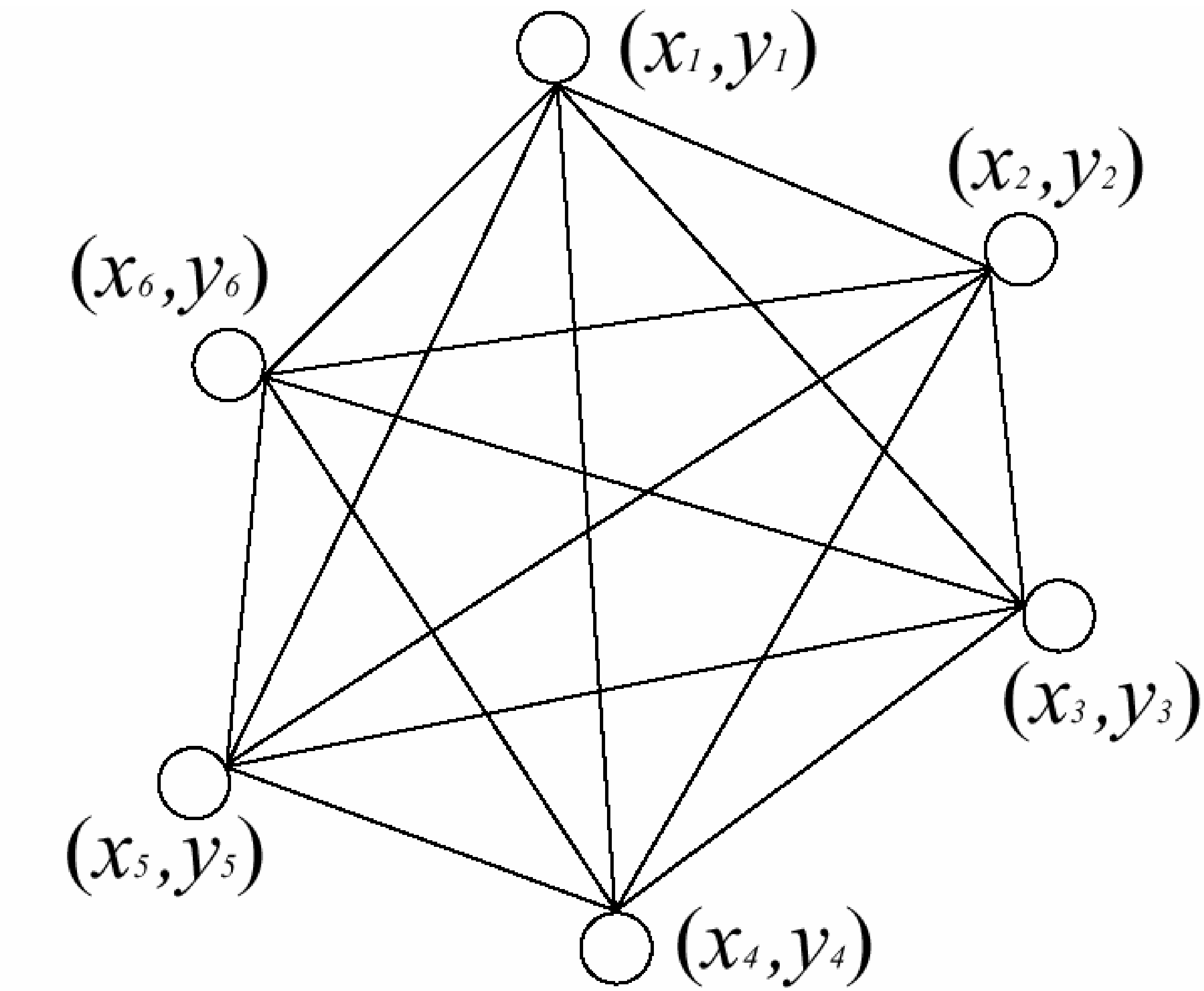
Clique Model

- Circuit hypergraphs corresponding to netlists are typically transformed into graphs.

- In the clique model, a k-pin net with the weight W is typically transformed into $k(k-1)/2$ two-pin nets with certain weights, $W/(k-1)$.

Clique Model

A six-pin net



Target Distance

$$\min_{(x_i, y_j)} \sum_{1 \le i < j \le N} c_{ij} d_{ij}$$

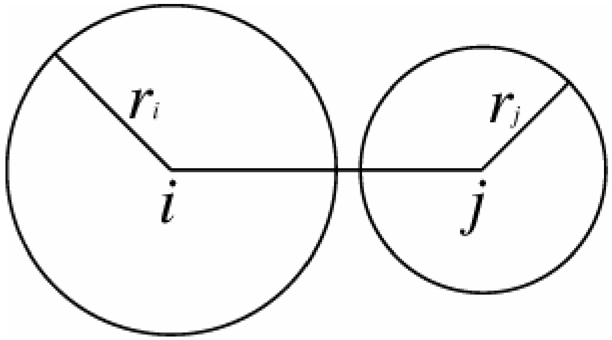
$$\text{s.t.} \quad r_i + r_j - d_{ij} \le 0$$

§ The objective function attempts to make distance as short as possible.

$$d_{ij} = \sqrt{(x_i - x_j)^2 + (y_i - y_j)^2}$$

§ The target distance between circles *i* and *j* is defined as

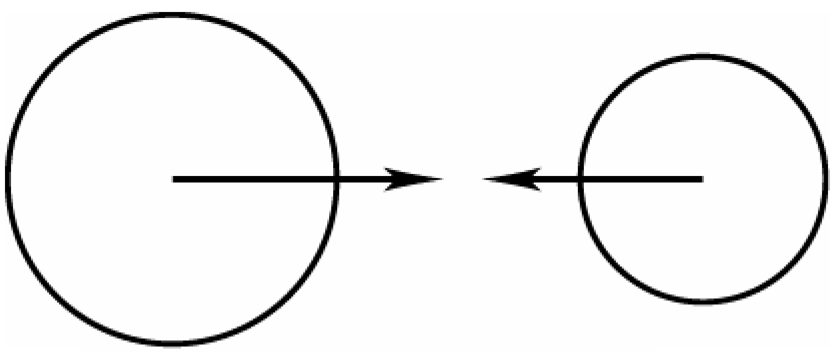
$$t_{ij} := \alpha (r_i + r_j)^2$$



Attractor-Repeller Mechanism

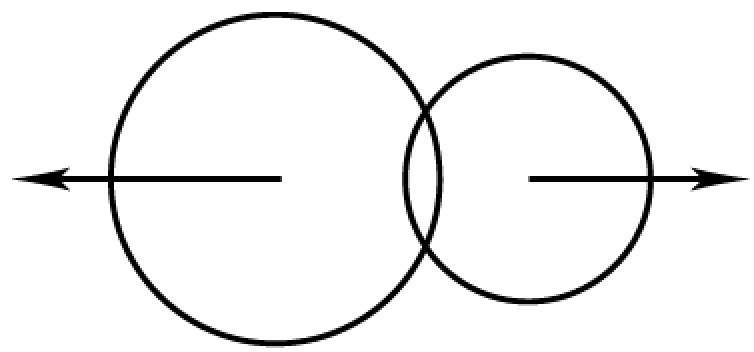
$$\min_{(x_i, y_j), w_F, h_F} \sum_{i,j \in M \cup P} c_{ij} D_{ij} + \sum_{i,j \in M} f\left(\frac{D_{ij}}{t_{ij}}\right)$$

$$f(z) = \frac{1}{z} - 1 \qquad D_{ij} = d_{ij}^2 = (x_i - x_j)^2 + (y_i - y_j)^2$$



$$r_i + r_j \leq d_{ij}$$

Attractive force



$$r_i + r_j > d_{ij}$$

Repulsive force

Convex AR Model

Define a convex function

$$F_{ij}(x_i, x_j, y_i, y_j) = \begin{cases} c_{ij}z + \frac{t_{ij}}{z} - 1, & z \geq T_{ij} \\ 2\sqrt{c_{ij}t_{ij}} - 1, & 0 \leq z < T_{ij} \end{cases}$$

$$T_{ij} = \sqrt{\frac{t_{ij}}{c_{ij} + \varepsilon}} \qquad z = (x_i - x_j)^2 + (y_i - y_j)^2$$

Model for the First Stage

$$\min_{(x_i,y_j),w_F,h_F} \sum_{i,j\in M\cup P} F_{ij}(x_i,x_j,y_i,y_j) - K\ln\left(\frac{D_{ij}}{T_{ij}}\right)$$

s.t.

$$x_i + r_i \le \frac{1}{2}w_F \ \text{ and } r_i - x_i \le \frac{1}{2}w_F, \ \text{ for all } i\in M,$$

$$y_i + r_i \le \frac{1}{2}h_F \ \text{ and } r_i - y_i \le \frac{1}{2}h_F, \ \text{ for all } i\in M,$$

$$w_F^{low} \le w_F \le w_F^{up},$$

$$h_F^{low} \le h_F \le h_F^{up}.$$

The Second Stage

Non-overlap constraints

$$\frac{1}{2}(w_i + w_j) \leq |x_i - x_j| \quad \text{if } |y_i - y_j| \leq \frac{1}{2}(h_i + h_j)$$
$$\frac{1}{2}(h_i + h_j) \leq |y_i - y_j| \quad \text{if } |x_i - x_j| \leq \frac{1}{2}(w_i + w_j)$$

Then

$$\frac{1}{2}(w_i + w_j) \leq \quad |x_i - x_j| \quad \text{or} \quad \frac{1}{2}(h_i + h_j) \leq \quad |y_i - y_j|$$

The Second Stage

$$\begin{cases} X_{ij} \geq \frac{1}{2}(w_i + w_j) - |x_i - x_j|, & X_{ij} \geq 0, \\ Y_{ij} \geq \frac{1}{2}(h_i + h_j) - |y_i - y_j|, & Y_{ij} \geq 0. \end{cases}$$

Then

$$\frac{1}{2}(w_i + w_j) \leq \quad |x_i - x_j| \quad \text{or} \quad \frac{1}{2}(h_i + h_j) \leq \quad |y_i - y_j|$$

is equivalent to

$$X_{ij} Y_{ij} = 0$$

Model for the Second Stage

Deadspace-free and overlap-free model

$$\min_{(x_i,y_i),w_i,h_i} \sum_{1 \le i < j \le n} c_{ij} L(x_i, x_j, y_i, y_j) + \gamma K X_{ij} Y_{ij}$$

s.t.

$$x_i + \frac{1}{2} w_i \le \frac{1}{2} w_F \quad \forall\, i,$$

$$y_i + \frac{1}{2} h_i \le \frac{1}{2} h_F \quad \forall\, i,$$

$$\frac{1}{2} w_i - x_i \le \frac{1}{2} w_F \quad \forall\, i,$$

$$\frac{1}{2} h_i - y_i \le \frac{1}{2} h_F \quad \forall\, i,$$

Plus...

Model for the Second Stage

$$w_i h_i = a_i \quad \forall\, i,$$

$$w_i^{low} \le w_i \le w_i^{up} \quad \forall\, i,$$

$$h_i^{low} \le h_i \le h_i^{up} \quad \forall\, i,$$

$$\delta\left(\frac{1}{2}(w_i + w_j) - |x_i - x_j|\right) \le X_{ij} \quad \forall\, 1 \le i < j \le n$$

$$X_{ij} \ge 0 \quad \forall\, 1 \le i < j \le n,$$

$$\delta\left(\frac{1}{2}(h_i + h_j) - |y_i - y_j|\right) \le Y_{ij} \quad \forall\, 1 \le i < j \le n,$$

$$Y_{ij} \ge 0 \quad \forall\, 1 \le i < j \le n$$

Minimization of Total Wire Length

§ To min ***rectilinear*** wire length (*Method A*)

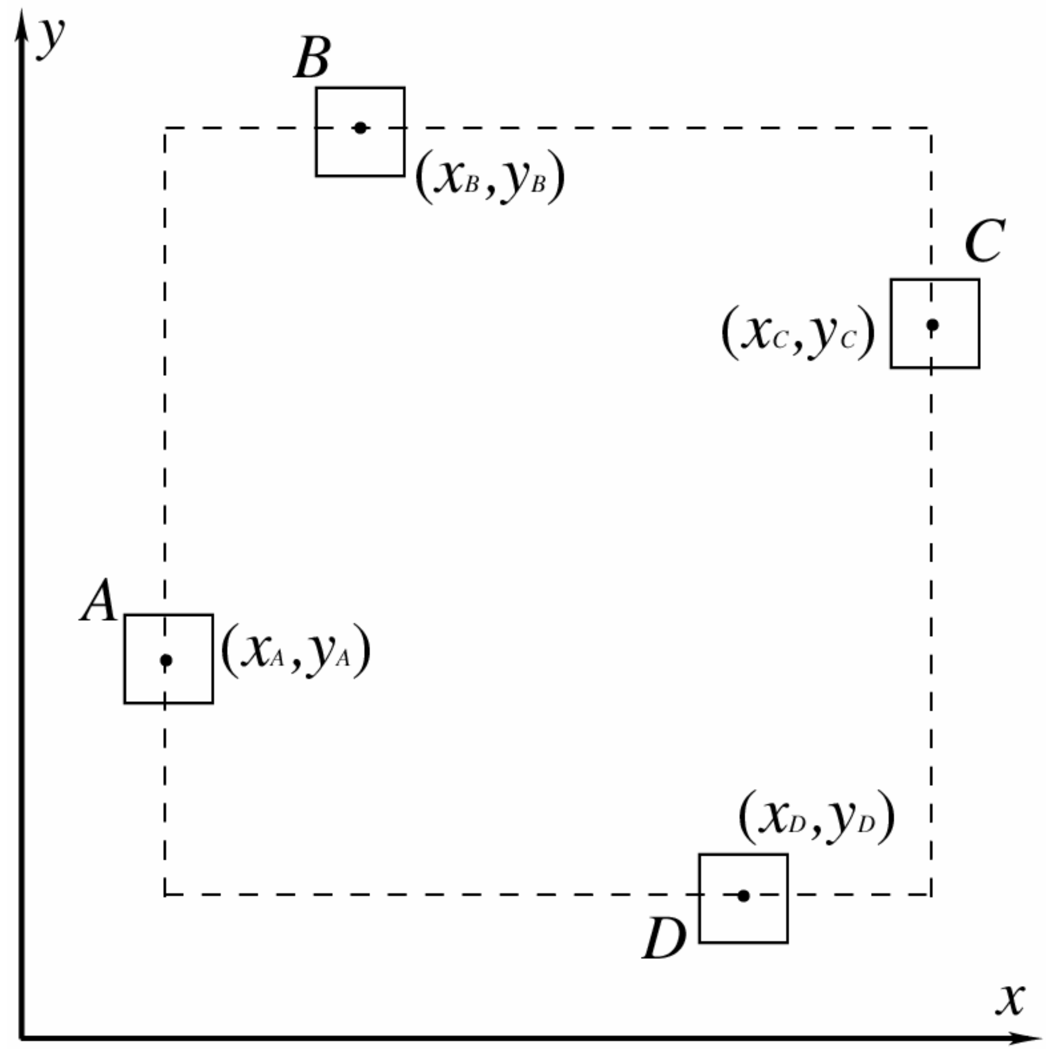
$$\sum_{\substack{i,j \in M \cup P \\ 1 \le i < j \le N}} c_{ij}(|x_i - x_j| + |y_i - y_j|) + KX_{ij}Y_{ij}$$

§ To min ***quadratic*** wire length (*Method B*)

$$\sum_{\substack{i,j \in M \cup P \\ 1 \le i < j \le N}} c_{ij}[(x_i - x_j)^2 + (y_i - y_j)^2] + KX_{ij}Y_{ij}$$

§ To minimize Half Perimeter Wire Length (HPWL) (*Method C*)

Minimization of the HPWL



An example of four-module nets with bounding box

Minimization of the HPWL

$$\min \quad \sum_{n=1}^{\#nets} c_n[(wl_x)_n + (wl_y)_n] + \sum_{\substack{i,j \in M \\ 1 \le i \le j < N}} KX_{ij}Y_{ij}$$

s.t.

$$(wl_x)_n \geq x_{m_1} - x_{m_2},$$

$$(wl_x)_n \geq x_{m_2} - x_{m_1},$$

$$\vdots$$

$$(wl_x)_n \geq x_{m_{t-1}} - x_{m_t},$$

$$(wl_x)_n \geq x_{m_t} - x_{m_{t-1}},$$

and

Minimization of the HPWL

$$(wl_y)_n \geq y_{m_1} - y_{m_2},$$

$$(wl_y)_n \geq y_{m_2} - y_{m_1},$$

$$\vdots$$

$$(wl_y)_n \geq y_{m_{t-1}} - y_{m_t},$$

$$(wl_y)_n \geq y_{m_t} - y_{m_{t-1}},$$

and

$$X_{ij} \geq 0 \qquad \forall 1 \leq i < j \leq N,$$

$$Y_{ij} \geq 0 \qquad \forall 1 \leq i < j \leq N.$$

Experimental Results (MINOS 5.5)

MCNC circuit	Total area (mm^2)	Our Methodology						
		Our area (mm^2)	Runtime			HPWL		
			Method A min/avg (s)	Method B min/avg (s)	Method C min/avg (s)	Method A min/avg (mm)	Method B min/avg (mm)	Method C min/avg (mm)
apte	46.56	46.56	0.093/0.69	0.084/1.04	0.11/0.94	384.30/425.09	386.81/436.59	397.70/438.82
xerox	19.35	19.35	0.34/1.23	0.33/2.03	0.25/0.98	420.11/462.12	433.27/475.87	427.61/469.75
hp	8.30	8.30	0.37/1.17	0.21/1.65	0.42/1.72	131.83/154.84	139.80/149.64	130.50/151.28
ami33	1.16	1.16	8.11/14.16	7.41/10.03	7.53/9.51	60.36/65.31	60.25/62.37	61.40/62.83
ami49	35.4	35.4	37.91/66.09	38.78/55.53	38.90/56.46	684.62/720.65	681.72/706.06	681.70/709.46

Experimental results with our methodology

Experimental Results (MINOS 5.5)

Comparison with *MK* model

MCNC circuit	Total area (mm^2)	MK [31] Area (mm^2)	Runtime (s)	HPWL (mm)
apte	46.56	46.55	789	344.36
xerox	19.35	19.50	1198	401.25
hp	8.30	8.83	1346	118.82
ami33	1.16	1.16	75684	53.39
ami49	35.4	35.58	612103	775.10

Results reported by *MK* (Murata and Kuh,1998)

Experimental Results (MINOS 5.5)

Comparison with *MK* model

MCNC circuit	Our Methodology vs *MK*					
	Speed-up			WL		
	Method *A* min	Method *B* min	Method *C* min	Method *A* min	Method *B* min	Method *C* min
apte	8483.87	9392.86	7172.73	-11.60%	-12.33%	-15.49%
xerox	3523.53	3630.30	4792.00	-4.70%	-7.98%	-6.57%
hp	3637.84	6409.52	3204.76	-10.95%	-17.66%	-9.83%
ami33	9332.18	10213.77	10051.00	-13.05%	-12.85%	-15.00%
ami49	16146.21	15783.99	15735.30	+11.67%	+12.05%	+12.05%
Average	8224.73	9086.09	8191.16	-5.73%	-7.75%	-6.97%

Improvements in Runtime and Wire Length Compared with *MK*

Experimental Results (MINOS 5.5)

Comparison with *AM* model

MCNC circuit	Total area (mm^2)	*AM* [1]		
		Area min/avg (mm^2)	Runtime avg (s)	WL min/avg (mm)
apte	46.56	46.97/48.95	15.4	464/560
xerox	19.35	19.51/20.62	20.1	373/468
hp	8.30	8.96/9.72	15.3	177/214
ami33	1.16	1.18/1.24	31.0	62.5/75.4
ami49	35.4	36.07/37.8	31.9	673/812

Results reported by *AM* (Adya and Markov, 2003)

Experimental Results (MINOS 5.5)

Comparison with *AM* model

MCNC circuit	Our Methodology vs *AM*					
	Speed-up			WL		
	Method *A* avg	Method *B* avg	Method *C* avg	Method *A* min/avg	Method *B* min/avg	Method *C* min/avg
apte	22.32	14.81	16.38	+17.18/+24.09%	+16.64/+22.04%	+14.29/+21.64%
xerox	16.34	9.90	20.51	-12.63/+1.26%	-16.16/-1.68%	-14.64/-0.37%
hp	13.08	9.27	8.90	+25.52/+27.65%	+21.02/+30.07%	+26.27/+29.31%
ami33	2.19	3.09	3.26	+3.42/+12.48%	+3.60/+17.28%	+1.76/+16.67%
ami49	0.48	0.57	0.57	-1.73/+9.22%	-1.29/+13.05%	-1.29/+12.63%
Average	10.88	7.53	9.92	+6.35/+14.94%	+4.76/+16.15%	+5.28/+15.97%

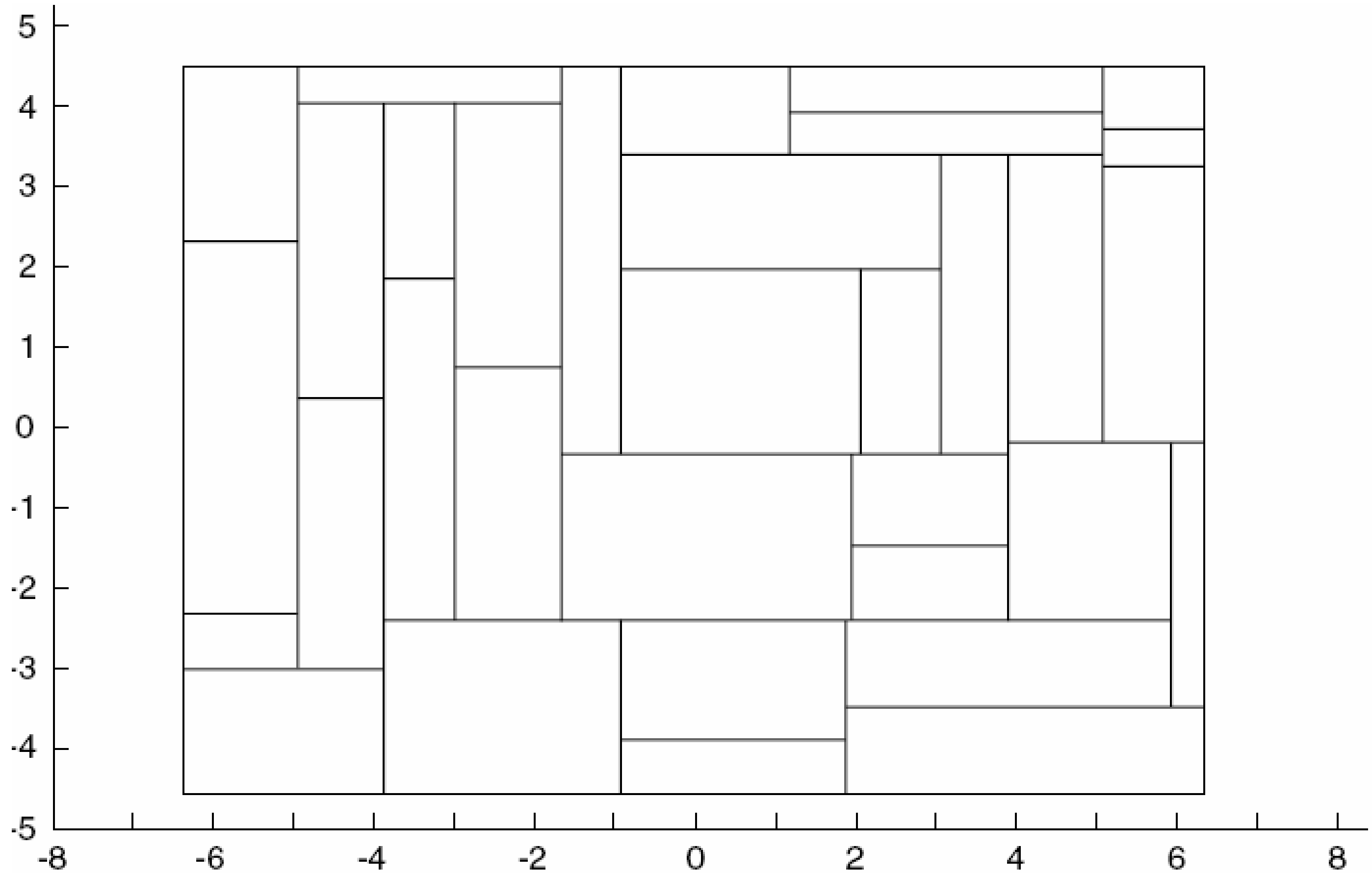
Improvements in Runtime and Wire Length Compared with *AM*

Deadspace in Layouts

MCNC circuit	Total area (mm^2)	MK [31] Area (mm^2)	MK [31] Deadspace	AM [1] Area min/avg (mm^2)	AM [1] Deadspace min/avg	Our Methodology Area (mm^2)	Our Methodology Deadspace min/avg Method A	Method B	Method C
apte	46.56	46.55	-0.02%	46.97/48.95	0.87%/4.88%	46.56	**0%/0%**	**0%/0%**	**0%/0%**
xerox	19.35	19.50	0.77%	19.51/20.62	0.82%/6.16%	19.35	**0%/0%**	**0%/0%**	**0%/0%**
hp	8.30	8.83	6.0%	8.96/9.72	7.40%/14.60%	8.30	**0%/0%**	**0%/0%**	**0%/0%**
ami33	1.16	1.16	0%	1.18/1.24	1.70%/6.45%	1.16	**0%/0.11%**	**0%/0.034%**	**0%/0.013%**
ami49	35.4	35.58	0.5%	36.07/37.8	1.86%/6.35%	35.4	**0%/0.11%**	**0%/0.063%**	**0%/0.094%**

Deadspace comparisons with *MK* and *AM*

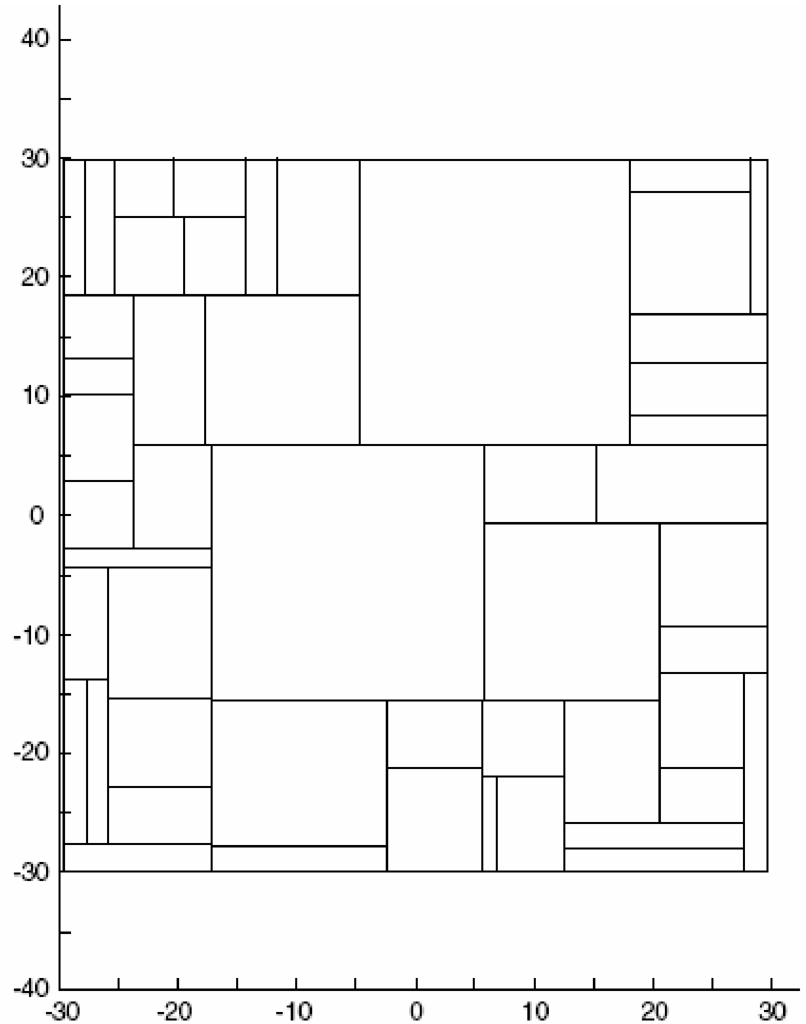
MCNC ami33 Layout



Floorplan for *ami*33 with HPWL = 62.65

$(\alpha = 1.02, \beta = 10, \gamma = 1.08, \delta = 1)$

MCNC ami49 Layout



Floorplan for *ami*49 with HPWL = 716.74
($\alpha = 0.15, \beta = 10, \gamma = 1, \delta = 0.128$)

Summary of Results

- The **zero deadspace** constraint is enforced (unlike *MK* and *AM*)
- The **running time** is significantly faster than *MK*
- The best achieved HPWL **total wire length** is (on average) better than *AM* model.

Conclusions

- The convex model is applied to *circuit* floorplanning.
- This is the ***first time*** that *fixed-outline* floorplanning is solved by using a convex optimization model.
- The results show very promising floorplanning quality (deadspace, running time and total wire length).

Thank you!